In the Claims:

1. (Original) A MOS transistor comprising:

a gate electrode on a substrate, the gate electrode having a first lateral protrusion extending from a lower portion of a first sidewall of the gate electrode and a second lateral protrusion extending from a lower portion of a second sidewall of the gate electrode;

a drain region in the substrate comprising a first lightly-doped drain region under the first lateral protrusion, a second lightly-doped drain region that is deeper than the first lightly-doped drain region adjacent the first lightly-doped drain region, and a heavily-doped drain region adjacent to the second lightly-doped drain region; and

a source region in the substrate comprising a first lightly-doped source region under the second lateral protrusion, a second lightly-doped source region that is deeper than the first lightly-doped source region adjacent the first lightly-doped source region, and a heavily-doped source region adjacent to the second lightly-doped source region.

2. (Original) The MOS transistor of Claim 1, further comprising an insulating gate spacer covering the first and second sidewalls of the gate electrode, wherein the second lightly-doped drain region and the second lightly-doped source region are under bottom portions of the insulating gate spacer.

3. (Original) The MOS transistor of Claim 2, wherein the heavily doped drain region is adjacent a first outer sidewall of the insulating gate spacer and wherein the heavily doped source region is adjacent a second outer sidewall of the insulating gate spacer.

4. (Original) The MOS transistor of Claim 1, wherein the gate electrode has an inverted T-shape.

5. (Original) The MOS transistor of Claim 1, further comprising a gate dielectric layer interposed between the gate electrode and the substrate.

6. (Original) The MOS transistor of Claim 2, further comprising a curing thermal oxide layer on the sidewalls of the gate electrode, the second lightly-doped drain region and the second lightly-doped source region.

7. (Original) The MOS transistor of Claim 6, wherein the insulating gate spacer is on the curing thermal oxide layer.

8. (Original) The MOS transistor of Claim 7, further comprising a spacer etch stop layer interposed between the insulating gate spacer and the curing thermal oxide layer.

9. (Original) The MOS transistor of Claim 1, wherein the sidewalls of the first and second lateral protrusions are vertically profiled.

10. (Original) The MOS transistor of Claim 1, wherein the sidewalls of the first and second lateral protrusions are sloped at positive angles.

11. (Original) The MOS transistor of claim 1 wherein the sidewalls of the first and second lateral protrusions are sloped at negative angles.

12. (Original) The MOS transistor of claim 1 further comprising a metal silicide layer on the upper surface of the gate electrode, the surface of the heavily-doped drain region and the surface of the heavily-doped source region.

13. (Original) A CMOS integrated circuit device comprising:

a semiconductor substrate having an NMOS transistor region and a PMOS transistor region therein;

an inverted T-shaped NMOS gate electrode on the NMOS transistor region;

an inverted T-shaped PMOS gate electrode on the PMOS transistor region;

first gate spacers on the sidewalls of the NMOS gate electrode;

second gate spacers on the sidewalls of the PMOS gate electrode;

a pair of first n-type lightly-doped regions in the substrate under portions of the NMOS gate electrode;

a pair of second n-type lightly-doped regions in the substrate, each of which is under a portion of the first gate spacers, the second n-type lightly-doped regions being deeper than the first n-type lightly-doped regions;

a pair of n-type heavily-doped regions in the substrate, each of which is adjacent to one of the second n-type lightly-doped regions; and

a pair of p-type heavily-doped regions in the substrate adjacent the PMOS gate electrode.

14. (Original) The CMOS integrated circuit device of Claim 13, wherein the NMOS gate electrode and the PMOS gate electrode are the same height above the substrate.

15. (Original) The CMOS integrated circuit device of Claim 13, further comprising a gate dielectric layer interposed between the NMOS gate electrode and the substrate and between the PMOS gate electrode and the substrate.

16. (Original) The CMOS integrated circuit device of Claim 15, wherein the depth of each of the second n-type lightly-doped regions is about the same as the combined depth of one of the first n-type lightly-doped regions, the gate dielectric layer and the crossbar portion of the NMOS gate electrode.

17. (Original) The CMOS integrated circuit device of Claim 13, wherein the sidewalls of the crossbar portion of the inverted T-shaped NMOS gate electrode are vertically profiled and wherein the sidewalls of the crossbar portion of the inverted T-shaped PMOS gate electrode are vertically profiled.

18. (Original) The CMOS integrated circuit device of Claim 13, wherein at least one of the sidewalls of the crossbar portion of the inverted T-shaped NMOS gate electrode is sloped at a positive angle and wherein at least one of the sidewalls of the crossbar portion of the inverted T-shaped PMOS gate electrode is sloped at a positive angle.

19. (Original) The CMOS integrated circuit device of Claim 13, wherein at least one of the sidewalls of the crossbar portion of the inverted T-shaped NMOS gate electrode is sloped at a negative angle and wherein at least one of the sidewalls of the crossbar portion of the inverted T-shaped PMOS gate electrode is sloped at a negative angle.

20. (Original) The CMOS integrated circuit device of Claim 13, further comprising a metal silicide layer on the upper surface of the NMOS gate electrode, the upper surface of the PMOS gate electrode, the n-type heavily-doped regions, and the p-type heavily-doped regions.

21. (Original) The CMOS integrated circuit device of Claim 13, further comprising an n-type pocket impurity region covering at least the sidewalls of the p-type heavily-doped regions, the n-type pocket impurity region being extended to the region under the PMOS gate electrode.

22. (Original) The CMOS integrated circuit device of Claim 13, further comprising a pair of first p-type lightly-doped regions in the substrate under portions of the PMOS gate

electrode and a pair of second p-type lightly-doped regions in the substrate, each of which is under a portion of the second gate spacers, each the second p-type lightly-doped region being deeper than the first p-type lightly-doped regions, shallower than the p-type heavily-doped regions, and interposed between one of the first p-type lightly-doped regions and one of the p-type heavily-doped regions.

23-53. (Cancelled)